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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,206	11/26/2003	Michael A. Gaynes	FR920030002US1	1205

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,206	GAYNES ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,10 and 22-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10 and 22-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 22, 23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba (US Pat. 6,313,521) in view of Hoffman (US Pat. 6,630,661).

Regarding claim 1, Fig. 5B of Baba shows a semiconductor package comprising:

a chip carrier [1] including a grounded pad on a first side of said chip carrier (col. 8, lines 17-35);

a semiconductor chip [2] coupled to said first side of said chip carrier;

a conductive lid [13; col. 7, lines 29-31] thermally coupled to said semiconductor chip wherein the entire length of said conductive lid is substantially parallel with said first side of said chip carrier; and

a conductive block [10; col. 7, lines 18-22] electrically coupled to said grounded pad and to said conductive lid (col. 8, lines 17-35).

Fig. 5B of Baba shows most aspects of the instant invention except "a conductive block having about the same dimensions as a discrete chip component." Fig. 7 of Hoffman shows a discrete chip [154] component having about the same dimensions as the conductive structure [156]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hoffman into the device of Baba in order

to have a discrete conductive structure having about the same dimensions as a discrete chip component for compact package.

Regarding claim 2, Fig. 5B of Baba shows that a solder (11; silver paste; col. 7, lines 18-22) connects said conductive structure and said grounded pad.

Regarding claim 3, Fig. 5B of Baba shows that said conductive structure electrically coupled to said grounded pad with an electrically conductive adhesive material (silver paste; col. 7, lines 18-22 and col. 8, lines 17-35).

Regarding claim 4, Fig. 5B of Baba shows that conductive structure is electrically coupled to said conductive lid with an electrically conductive adhesive material (14; silver paste; col. 8, lines 17-35).

Regarding claim 5, Fig. 5B of Baba shows that said conductive structure is coupled to said chip carrier using an electrically insulative adhesive material (insulating epoxy resin; col. 8, lines 29-35).

Regarding claim 6, Fig. 5B of Baba shows that said conductive structure is coupled to said chip carrier using a thermally conductive adhesive material (11; silver paste; col. 7, lines 18-22).

Regarding claim 22, Fig. 5B of Baba shows an end of said conductive lid extends beyond at least one side of said semiconductor.

Regarding claim 23, Fig. 5B of Baba shows the conductive structure is located on the first side of the chip carrier.

Regarding claim 25, Fig. 5B of Baba shows that said conductive structure occupies a substantial amount of a gap between a lower surface of said conductive lid and an upper surface of said chip carrier.

Regarding claim 26, the combination of Baba/Hoffman fails to show "said conductive structure occupies about 90% of said gap." However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the conductive structure occupying about 90% of said gap in order to reduce the package size since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 1, 10 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jimarez et al. (US Pat. 6,407,334), hereinafter Jimarez in view of Hoffman (US Pat. 6,630,661).

Regarding claim 1, Fig. 10 of Jimarez shows a semiconductor package comprising:

a chip carrier [10] including a grounded pad on a first side of said chip carrier (Abstract);

a semiconductor chip [34] coupled to said first side of said chip carrier;

a conductive lid [46] thermally coupled to said semiconductor chip wherein the entire length of said conductive lid is substantially parallel with said first side of said chip carrier; and

a conductive block [26, 36] electrically coupled to said grounded pad and to said conductive lid (Abstract).

Fig. 10 of Jimarez shows most aspects of the instant invention except "a discrete conductive structure having about the same dimensions as a discrete chip component." Fig. 7

of Hoffman shows a discrete chip [154] component having about the same dimensions as the conductive block [156]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hoffman into the device of Jimarez in order to have a discrete conductive structure having about the same dimensions as a discrete chip component for compact package.

Regarding claim 10, Fig. 10 of Jimarez shows that a solder couples said conductive structure to said grounded pad (col. 2, lines 40-43), an electrically conductive adhesive material [42] couples said conductive structure to said conductive lid; and an electrically insulative adhesive material couples [18; col. 2, lines 14-16]] said conductive structure to the chip carrier.

Regarding claim 24, the combined teachings of Jimarez and Hoffman would show that said conductive structure has about the same dimensions as a surface mount technology (SMT) discrete component since Fig. 7 of Hoffman shows a discrete chip [154] component having about the same dimensions as the conductive structure [156].

Claims 27-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jimarez in view of Hoffman and Glenn et al. (US 6562655), hereinafter Glenn.

Regarding claim 27, Fig. 10 of Jimarez shows a semiconductor package comprising:

a chip carrier [10] including a grounded pad on a first side of said chip carrier (Abstract);

a semiconductor chip [34] coupled to said first side of said chip carrier;

a conductive lid [46] thermally coupled to said semiconductor chip wherein the entire length of said conductive lid is substantially parallel with said first side of said chip carrier; and

a conductive element [26, 36] electrically coupled to said grounded pad and to said conductive lid (Abstract).

Fig. 10 of Jimarez shows most aspects of the instant invention except a discrete conductive element/spring having about the same dimensions as a discrete chip component. Fig. 7 of Hoffman shows a discrete chip [154] component having about the same dimensions as the conductive block [156]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hoffman into the device of Jimarez in order to have a discrete conductive element having about the same dimensions as a discrete chip component for compact package.

The combination of Jimarez/Hoffman shows substantially the entire claimed structure except "a conductive spring." Fig. 6 of Glenn shows a semiconductor with a conductive structure comprising a spring [150]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Glenn into the device of Baba/Hoffman in order to have a conductive structure comprising a spring to secure the conductive lid.

Regarding claims 28-30, Fig. 10 of Jimarez shows that a solder couples the conductive element to the grounded pad (col. 2, lines 40-43), an electrically conductive adhesive material [42] couples said conductive element to said conductive lid; and an electrically insulative adhesive material couples [18; col. 2, lines 14-16]] said conductive element to the chip carrier.

Regarding claim 31, Fig. 10 of Jimarez shows the conductive element is coupled to said chip carrier using a thermally conductive adhesive material (solder).

Regarding claim 32, the combined teachings of Jimarez/Hoffman/Glenn would show that said conductive spring has about the same dimensions as a surface mount technology (SMT) discrete component since Fig. 7 of Hoffman shows a discrete chip [154] component having about the same dimensions as the conductive structure [156].

Regarding claim 33, Fig. 10 of Jimarez shows the conductive element occupies a substantial amount of a gap between a lower surface of said conductive lid and an upper surface of said chip carrier.

Response to Arguments

Applicant's arguments filed September 4, 2007 have been fully considered but they are not persuasive.

Applicants argue that " ... Rather, Applicants respectfully submit that Baba discloses an auxiliary board 10 which is a rectangular shaped with an opening (see Fig. 3 of Baba) so that auxiliary board 10 surrounds space 9 in which the semiconductor chip 2 and the chip components 7 are mounted (see column 7, lines 15-18 of Baba). ... Thus, Applicants respectfully submit that Baba provides no disclosure, teaching or motivation of a semiconductor package comprising a conductive block as claimed by Applicants." Examiner disagrees. Note that a conductive block can be any conductive structure since it implies that any solid piece of a hard substance that is conductive. Therefore, Baba's conductive ring of copper is a conductive block. Furthermore, Jimarez also shows a conductive block.

Applicants further argue that "Applicants respectfully submit that Hoffman would not provide any motivation, teaching or suggestion to combine with Baba since Hoffman discloses

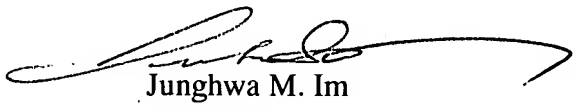
discrete structures so the combination of Baba and Hoffman would result in a plurality of discrete structures with spaces between each of the structures surrounding the semiconductor chip 2 and the chip components 7 resulting in the escape of electromagnetic waves. Applicants also note that auxiliary board 10 of Baba has a length and width which exceeds corresponding dimensions of semiconductor chip 2 so the auxiliary board 10 can not have the dimensions of a discrete chip component as taught by Hoffman. Thus, Applicants respectfully submit that Hoffman does not remedy the deficiencies in Baba since Baba requires a solid, continuous structure that exceeds the dimensions of a discrete chip component to surround the semiconductor chip 2 in order to prevent the escape of electromagnetic radiation." This is not persuasive. Firstly, note that the instant invention discloses that the conductive lid is needed to over come EMI sensitivity, therefore, this argument merely implies that "a plurality of discrete conductive structures with spaces" in the instant invention would also result in "the escape of electromagnetic waves." Secondly, note that the instant invention recites the limitation "a conductive block having about the same dimensions as a discrete chip component. " Note that "a discrete chip component" can have any dimensions. Therefore, this limitation merely implies that a conductive block can have any dimensions/sizes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Junghwa M. Im
Examiner
Art Unit 2811

jmi
9/10/2007